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PATENT

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AS/1765  
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LV 7/10/04

In Re U.S. Patent Application

Applicant: Lahnor, Peter et al.

Serial No.: 09/933,304

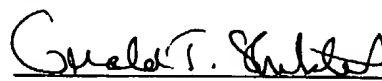
Filed: August 20, 2001

For: **CMP PROCESS**

Examiner: Vinh, Lan

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) Art Unit: 1765  
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) Confirmation No. 5680  
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Gerald T. Shekleton Reg. No. 27,466

**AMENDMENT**

Mail Stop AMENDMENT  
Commissioner for Patent  
P.O. Box 1450  
Alexandria, Virginia 22313-1450

Sir:

The Office Action of May 17, 2004 has been carefully reviewed and the following amendments and remarks are made in response thereto.

- As a result of excessively short polishing in the CMP process, metal residues in the following metal plane can lead to short circuits.

5 - Defects in underlying planes (e.g. scratches, holes) are mapped in the dielectric and are filled with metal. This metal can only be removed with difficulty in the CMP step and later leads to short circuits.

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The disadvantages listed are aggravated by the fact that the end point identification of the CMP process is unreliable. If the dielectric has a residual topology, then this results in further disadvantages since a longer polishing time becomes necessary.

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Methods of this type can also be applied to an interconnect plane, the so-called damascene technique being used. In this document, the technical subject matter is essentially described with reference to contact holes.

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The invention is based on the object of providing an improved CMP process.

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[ This object is achieved by means of the process in accordance with claim 1. ]

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The invention is based on the insight that the CMP process can be significantly improved by means of a suitable auxiliary layer which is applied to the dielectric before the contact hole or metal track etching. The auxiliary layer, which can be etched wet-chemically without any residues due to the oxidizing conditions during the metal CMP process or can be removed to a great extent by the polishing, reduces excessive processing of the surface of the dielectric.

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